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Silicon Labs Eliminates Jitter with Industry's Easiest-to-Use Clock Cleaner IC

Highly Integrated Si5317 Jitter Attenuating Clock Filters Unwanted Noise from High-Speed Networking and Telecommunications Systems

AUSTIN, Texas, Jun 14, 2010 (BUSINESS WIRE) -- Silicon Laboratories Inc. (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today announced the industry's most frequency-flexible timing IC solution for networking and telecommunications applications that require jitter attenuation for clock signals without clock multiplication. Silicon Labs' new Si5317 pin-controlled jitter cleaning clock IC provides jitter filtering to remove unwanted noise and produces low jitter outputs for a wide range of applications such as wireless backhaul equipment, DSLAMs, multi-service access nodes (MSANs), GPON/EPON optical line termination (OLT) line cards, and 10 GbE switches and routers.

As networking and telecom hardware designs migrate to higher speeds and greater complexity, timing architecture has become a key consideration in the overall system design. Managing clock jitter is especially critical in high-speed applications since this noise degrades overall system performance, impacting the design's bit-error-rate (BER) and signal-to-noise ratio (SNR). The Si5317 clock cleaner provides a simple, flexible and cost-effective jitter filtering solution for these performance-sensitive applications.

The Si5317 effectively removes unwanted noise on any clock frequency from 1 to 710 MHz and produces two ultra-low jitter output clocks at the same frequency as the input. Unlike traditional clock ICs or discrete phase-locked loop (PLL) module solutions requiring multiple components to support different frequencies, one Si5317-based design and layout supports jitter attenuation for any <710 MHz clock signal, enabling design reuse across multiple applications. Designers can use simple pin settings to configure the frequency range and PLL bandwidth, eliminating the need for firmware and serial programming required by traditional clock IC solutions.

"The Si5317 is the industry's most versatile and user-friendly jitter attenuating clock cleaner, providing an ultra-low jitter solution for high-performance and cost-sensitive access and networking applications that require exceptionally clean clocks," said Mike Petrowski, general manager of Silicon Labs' timing products. "The Si5317 simply drops into the clock path to provide jitter attenuation on clock signals up to 710 MHz without requiring firmware configuration or BOM modifications to accommodate different frequencies."

Based on Silicon Labs' patented DSPLL(R) architecture, the Si5317 clock cleaner delivers best-in-class jitter performance (0.29 ps RMS), improving BER and SNR in jitter-sensitive applications. This exceptional jitter performance - typically one-third lower jitter than competing clock ICs with integrated oscillators - enables a significant portion of the system jitter budget to be allocated to other devices, simplifying component selection and clock tree design.

The Si5317 integrates a single supply voltage regulator with excellent power supply noise rejection. This streamlined power supply design eliminates the need for multiple supply rails and discrete ferrite beads. On-chip power regulation also minimizes the board design's sensitivity to high-speed noise and switching power supplies, reducing the risk that the power supply noise might impact the design's overall jitter performance.

As the industry's most highly integrated jitter cleaning clock, the Si5317 requires no external PLL components, simplifying PCB design and layout in space-constrained applications while minimizing the threat of board-level noise impacting jitter performance. On-chip DSPLL technology eliminates the need for a charge pump and/or loop filter design required by traditional VCXO-based PLL modules and clock ICs. This high level of integration minimizes design time and development risk by guaranteeing loop stability and jitter performance across temperature, process and voltage variation. Combining all PLL components into a single device also eliminates sensitive noise entry points between discrete PLL components, improving immunity to board-level noise.

In addition to jitter attenuating clocks, Silicon Labs' broad portfolio of mixed-signal timing ICs includes programmable XO/VCXOs, CMOS-based silicon oscillators, high-performance clock generators, low jitter clock multipliers, buffers and physical layer timing devices. The Si5317 clock cleaner can be combined with many of these timing devices to enable a complete, ultra-low jitter timing solution. Companion timing IC products for the Si5317 include the Si500 silicon oscillator, the Si5338/34 <710 MHz differential clock generators, the Si5355/56 <200 MHz CMOS clock generators and the Si5330 low jitter clock buffers. The Si5317 easily connects to any of these timing ICs to provide two ultra-low jitter output clocks.

Pricing and Availability

Samples and production quantities of the Si5317 clock cleaner are available now. Pricing in 10,000-unit quantities begins at $6.00 (USD). The Si5317-EVB evaluation board is available now for $125 (USD), providing a high-performance, user-configurable platform for evaluating the Si5317 jitter cleaning clock. For more information about the Si5317, please visit www.silabs.com/pr/clocks.

Silicon Laboratories Inc.

Silicon Laboratories is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs' diverse portfolio of highly integrated, easy-to-use products offers customers significant advantages in performance, size and power consumption. These patented solutions serve a broad set of markets and applications including consumer, communications, computing, industrial and automotive.

Headquartered in Austin, TX, Silicon Labs is a global enterprise with operations, sales and design activities worldwide. The company is committed to contributing to our customers' success by recruiting the highest quality talent to create industry-changing innovations. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

This press release may contain forward-looking statements based on Silicon Laboratories' current expectations. These forward-looking statements involve risks and uncertainties. A number of important factors could cause actual results to differ materially from those in the forward-looking statements. For a discussion of factors that could impact Silicon Laboratories' financial results and cause actual results to differ materially from those in the forward-looking statements, please refer to Silicon Laboratories' filings with the SEC. Silicon Laboratories disclaims any intention or obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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