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Silicon Labs Addresses Optical Networking Challenges with Industry's First High-Performance 4-PLL Clock ICs

Si537x Timing ICs Offer Highest Performance, Highest Integration and Lowest Jitter Available for Optical Transport Network Multiservice Platforms

AUSTIN, Texas--(BUSINESS WIRE)-- Silicon Laboratories Inc. (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today introduced the industry's highest performance, most integrated clock ICs available to address the complex timing requirements of high-speed optical transport network (OTN) applications. Leveraging Silicon Labs' patented DSPLL® technology, the new Si5374 and Si5375 clocks are the first single-chip timing ICs to integrate four independent, high-performance phase locked loops (PLLs), providing twice the PLL integration and 40 percent lower jitter than competing solutions

OTN is a next-generation protocol (ITU G.8251 and G.709) that provides an efficient way to multiplex different services onto optical networks, making it an ideal solution for edge routers, wavelength division multiplexing (WDM) transmission equipment, Carrier Ethernet and multi-service platforms. OTN applications pose complex timing challenges by requiring multiple low-jitter clocks at non-integer-related frequencies. Silicon Labs' quad-DSPLL Si537x devices produce up to eight low-jitter output clocks, simplifying the design of any-protocol, any-port 10G, 40G and 100G OTN line cards.

Each DSPLL clock multiplier can be configured to generate any frequency from 2 kHz to 808 MHz from a 2 kHz to 710 MHz input. This exceptional frequency flexibility reduces the cost and complexity of multi-protocol OTN line cards by minimizing the need for multiple jitter-cleaning clock ICs. The Si537x devices' flexible DSPLL architecture simplifies the generation of high-speed PHY reference clocks with industry-leading jitter performance of 0.4 picoseconds, eliminating the need for discrete VCXO-based PLLs currently used in OTU3 and OTU4 applications.

The Si537x devices can reliably lock to gapped clock inputs — a critical OTN line card clock requirement — without separate upstream low-bandwidth PLLs. Other carrier-grade features include SONET-compatible jitter peaking (0.1 dB max) and an innovative hitless switching capability that minimizes output clock phase transients during reference switching, producing a 25x smaller phase transient than competing solutions. Each DSPLL engine features a fully integrated loop filter that supports user-programmable bandwidths as low as 4 Hz, enabling wander filtering in addition to jitter attenuation, configurable on a per channel basis.

"The convergence of high-bandwidth data, video and voice services over OTN and increasing optical line card port densities require higher levels of clock integration and ultra-low jitter to minimize design cost and complexity," said Mike Petrowski, general manager of Silicon Labs' timing products. "Silicon Labs' new Si537x clock ICs offer more high-performance PLL integration than competing solutions at the industry's lowest jitter levels, setting a new benchmark for purpose-built OTN clocking solutions."

The Si5374 device has eight input clocks and eight output clocks while the Si5375 offers four input clocks and four output clocks for applications requiring fewer clocks. With its quad-DSPLL configuration, a single Si5374 clock can generate different frequencies simultaneously, enabling the design to support SONET/SDH, 1/10/100G Ethernet, 1/2/4/8/10G Fibre Channel, 3G/HD SDI video and other protocols simultaneously in the same device.

The Si537x clocks provide a smooth upgrade path for existing customers migrating from Silicon Labs' Si5319/26 jitter-attenuating clocks to a more integrated jitter-cleaning clock solution designed to minimize BOM cost and complexity. The Si537x clocks effectively replace four timing devices with a single IC in high-port-count 10G/40G/100G OTN line cards.

Pricing and Availability

Samples and production quantities of the Si537x clock ICs are available now. Si537x clock prices range from $39 to $59 in 10,000-unit quantities. The Si5374-EVB and Si5375-EVB evaluation kits are available for $350 each. (All prices are in USD.) For more information, please visit http://www.silabs.com/pr/clocks.

Silicon Laboratories Inc.

Silicon Laboratories is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed

by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs' diverse portfolio of patented semiconductor solutions offers customers significant advantages in performance, size and power consumption. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

This press release may contain forward-looking statements based on Silicon Laboratories' current expectations. These forward-looking statements involve risks and uncertainties. A number of important factors could cause actual results to differ materially from those in the forward-looking statements. For a discussion of factors that could impact Silicon Laboratories' financial results and cause actual results to differ materially from those in the forward-looking statements, please refer to Silicon Laboratories' filings with the SEC. Silicon Laboratories disclaims any intention or obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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