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Silicon Labs Simplifies Data Center Timing with PCI Express Buffers

Si531xx and Si53019 PCIe Gen3 Fanout Buffers Minimize Power and External Components for Server and Storage Motherboard Designs

AUSTIN, Texas--(BUSINESS WIRE)-- [Silicon Labs](#) (NASDAQ: SLAB), a leading provider of high-performance timing solutions for [Internet infrastructure](#), today introduced a new family of PCI Express (PCIe) Gen1/2/3 fanout buffers designed for data center applications including servers, storage and switches. Designed for today's leading x86 motherboard and server systems, the new Si5310x/11x/019 PCIe buffer family expands Silicon Labs' growing [PCIe timing portfolio](#) with the industry's most power-efficient fanout buffers. Available with a broad choice of output count options, the new PCIe buffers are qualified for use in 98 percent of x86-based server/storage motherboard designs.

For many years, data center equipment makers have had a limited supplier base for PCIe Gen3 buffers approved by the leading x86 CPU and chipset supplier. These conventional PCIe buffers are based on power-hungry constant-current output technology, which increases bill of materials (BOM) count by requiring four external termination resistors per output, as well as one reference resistor. As power consumption and cooling costs have become critical concerns for data center designs, developers increasingly are seeking components that deliver the utmost energy efficiency while complying with stringent x86 board specifications. Silicon Labs' Si5310x/11x/019 family provides equipment makers with lower power, standards-compliant PCIe buffer products qualified by the leading x86 CPU and chipset supplier and backed by an outstanding technical support organization.

More than 90 percent of existing motherboard designs use PCIe buffers based on constant-current output technology. To address this existing market need, Silicon Labs' new Si53019 PCIe constant-current buffer delivers a fully qualified drop-in compatible solution with 30 percent lower power than conventional solutions.

To minimize power even further, Silicon Labs' Si5310x and Si5311x devices use an innovative push-pull output architecture to deliver the industry's lowest power family of PCIe buffers. These devices consume 60 percent less power than constant-current buffers while reducing the required number of external resistors per output, significantly reducing external component count and simplifying printed circuit board (PCB) design. For example, by using Silicon Labs' 19-output Si53119 push-pull buffer instead of a conventional constant-current device, developers can save nearly 1 Watt of power and eliminate 39 external components.

Silicon Labs' Si5310x and Si5311x push-pull output devices are also optimal PCIe timing solutions for system designs using new ARM®-based SoCs targeting the hyperscale server and storage markets. Similar to x86-based designs, ARM-based SoC platforms for the server and storage markets use PCIe as the primary system data bus and interconnect. With system-level power efficiency being a major benefit of the hyperscale architecture, the new Si5310x and Si5311x push-pull output devices are ideally suited for all server and storage platform designs, regardless of CPU architecture.

In addition to power consumption concerns, data center equipment makers face the challenge of maintaining signal integrity while driving clocks between boards over cables up to 60 inches in length. A PCIe clock's rise and fall times degrade and slow down over such long distances, resulting in reduced jitter performance and increased system packet loss failures. Silicon Labs' PCIe Gen3 buffers are designed to drive long clock signal traces while maintaining standards-compliant PCIe rise and fall time specifications to prevent excessive jitter and packet loss.

Silicon Labs' new PCIe buffer family includes 6, 8, 12, 15 and 19-output devices as well as a combination of constant-current and push-pull buffers, enabling developers to tailor the optimal solution for each application. Silicon Labs' devices are pin- and functionally compatible replacements for conventional PCIe buffers, providing developers with superior alternatives that improve power efficiency, signal integrity and jitter performance.

"Mobile Internet traffic and cloud computing are driving the need for faster, higher performance data center equipment requiring high-precision timing solutions supporting both the PCIe standard and leading x86 specifications," said James Wilson, marketing director for Silicon Labs' timing products. "We've expanded our PCIe timing portfolio to include fully x86-qualified PCIe Gen3 fanout buffers that reduce the power, cost and complexity of data center equipment. Our new PCIe products complement Silicon Labs' any-frequency clock generators by providing a single-chip clock tree solution for any server, switch or storage design."

Silicon Labs offers a [broad timing portfolio](#) of frequency-flexible clock generators, jitter attenuators, clock buffers, PCIe clocks

and oscillators to address a wide range of Internet infrastructure applications. These high-performance timing solutions enable developers to work with a single one-stop-shop supplier capable of fulfilling comprehensive timing requirements in data center, core network, wireless infrastructure, broadband access, and test and measurement designs.

Pricing and Availability

Samples and production quantities of the Si531xx and Si53019 PCIe fanout buffers are available now. Pricing for the Si531xx push-pull output buffers begins at \$1.70 in 10,000-unit quantities, and the Si53019 constant-current output buffer is priced at \$2.85 in 10,000-unit quantities (all prices in USD). To accelerate development of server and storage applications based on push-pull output clock buffers, Silicon Labs offers the Si53108-EK, Si53112-EK and Si53119-EK evaluation boards, each priced at \$125 (USD MSRP). For more information about Silicon Labs' PCIe Gen3 fanout buffers and to purchase samples and development tools, please visit www.silabs.com/PCI-express-clocks.

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