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Silicon Labs Introduces Low-Jitter Clock Buffers with Industry's Highest Integration of Clock Tree Functions

Si533xx Clock Buffers Replace Discrete Components and Provide Universal Format Translation to Simplify System Design

AUSTIN, Texas--(BUSINESS WIRE)-- Silicon Laboratories Inc. (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today introduced the industry's first universal clock buffers capable of replacing LVPECL, LVDS, CML, HCSL and LVCMOS buffers with a single IC, eliminating the need for multiple fixed-format buffers. The new Si533xx family integrates common clock tree functions including clock distribution, clock muxing, clock division, format translation and level translation. Based on a patented low-phase-noise clock driver architecture, the Si533xx family features ultra-low additive jitter with guaranteed maximum jitter specifications, simplifying clock tree design and providing designers more jitter margin for other devices. The Si533xx clock buffers are purpose-built to address the demanding requirements of communications, data center, wireless infrastructure, broadcast video and embedded computing applications.

The Si533xx clock buffer family is part of Silicon Labs' comprehensive portfolio of timing devices, enabling customers to simplify both the design and procurement of complete clock tree solutions for virtually any high-performance application. Silicon Labs-based clock trees provide the industry's highest level of integration, minimizing the number of components necessary for clock generation and distribution. By being able to source all timing components from a single supplier, end-to-end performance can be guaranteed, eliminating interoperability headaches while simplifying the customer's supply chain.

Competing clock buffers support only a single-output signal format and do not integrate basic clock tree functions. This deficiency forces system designers to use a variety of discrete buffers, muxes, dividers and level translators to address their clock distribution requirements, adding complexity and cost to their designs. Silicon Labs' flexible and highly integrated solution resolves these issues, adding flexibility, simplifying clock trees, reducing design complexity and eliminating procurement headaches.

The Si533xx clock buffers provide a single-chip solution that replaces differential LVPECL, LVDS, CML and HCSL buffers with up to 10 outputs, LVCMOS buffers with up to 20 outputs, and discrete muxes, dividers and level translators. The unique architecture of the Si533xx clock buffers maximizes design flexibility. Clock outputs are split into two independent banks. The signal format of each bank is user-selectable through simple pin-strapping, providing developers with an array of options. Both banks have dedicated supply voltage pins independent of the core voltage, enabling simple voltage-level translation. The devices' universal input stage accepts two differential or single-ended inputs, and a low-noise 2:1 input mux supports glitchless switching, eliminating the risk of runt pulses being transferred to the device outputs during an input clock switch. In addition, some Si533xx buffers support individual output enable pins for each output clock, providing control flexibility.

The Si533xx family was designed to provide a high level of integration and flexibility without compromising performance. The Si53302 device is the industry's lowest jitter multi-format buffer (100 fs RMS typical), providing performance comparable to best-in-class fixed-format buffers. In addition, the device's 2:1 input mux provides more than 60 dB of noise isolation between clock inputs, significantly minimizing cross-talk-induced jitter and guaranteeing low noise operation in applications requiring two input clocks. On-chip supply voltage regulation provides high power supply noise rejection, ensuring robust low-jitter operation alongside FPGAs, ASICs, SoCs and PHYs.

"We've applied innovative mixed-signal techniques to create an entirely new category of clock buffers specifically designed to address the headaches typically associated with clock tree design," said Mike Petrowski, vice president and general manager of Silicon Labs' timing products. "The Si533xx family redefines clock buffer functionality by encompassing a high level of integration and universal, any-format translation without performance compromises, giving developers greater flexibility to innovate and simplify their system designs."

Pricing and Availability

Volume production quantities of Silicon Labs' Si533xx clock buffers are available now in a variety of package types beginning at $0.80 (USD) in 10,000-unit quantities. The Si533xx family is supported by the Si53301/4-EVB development kit populated with a 2-input, 6-output Si53301 universal buffer/translator. This development kit can be used to evaluate the performance of all Si533xx products and is easily configured via jumpers with no external software required.

Silicon Labs also provides an online cross reference tool to identify footprint-compatible and functionally equivalent Si533xx buffers that are replacements for traditional buffer devices. Visit http://www.silabs.com/support/pages/cross-reference.aspx.

For additional clock buffer product information, samples and development tools, please visit www.silabs.com/timing.

Silicon Laboratories Inc.

Silicon Laboratories is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs' diverse portfolio of patented semiconductor solutions offers customers significant advantages in performance, size and power consumption. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

This press release may contain forward-looking statements based on Silicon Laboratories' current expectations. These forward-looking statements involve risks and uncertainties. A number of important factors could cause actual results to differ materially from those in the forward-looking statements. For a discussion of factors that could impact Silicon Laboratories' financial results and cause actual results to differ materially from those in the forward-looking statements, please refer to Silicon Laboratories' filings with the SEC. Silicon Laboratories disclaims any intention or obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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Silicon Laboratories Inc.
Dale Weisman, +1-512-532-5871
dale.weisman@silabs.com

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