Q4 Company

ASE launches its Integrated Design EcosystemTM to enable silicon package design efficiencies that reduce cycle time by half

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SUNNYVALE, Calif.--(BUSINESS WIRE)-- Advanced Semiconductor Engineering, Inc. (ASE), a member of ASE Technology Holding Co., Ltd. (NYSE: ASX, TAIEX: 3711), today announced the launch of its Integrated Design EcosystemTM (IDE), a collaborative design toolset optimized to systematically boost advanced package architecture across its VIPackTM platform. This innovative approach allows a seamless transition from single die SoC to multi-die disaggregated IP blocks including chiplets and memory for integration using 2.5D or advanced fanout structures. ASE's IDE enables design efficiencies up to 50% and sets new standards for quality and user experience. Integrating novel package design tool capabilities into ASE's workflow has resulted in significant cycle time reduction while lowering customer costs.

Enhanced features of IDE include cross platform interaction encompassing layout and verification, advanced RDL and silicon interposer auto routing with embedded design rule checking (DRC), and Package Design Kit (PDK) implementation in the design workflow. As an example, a critical milestone has been achieved for a Fan Out Chip on Substrate - Chip Last (FOCoS-CL) package where the design cycle timeline has been substantially reduced from 90 days to 45 days.

Today's semiconductor technology roadmaps comprise complex performance requirements that are driving advanced packaging trends, yet present unique package design challenges. Frontline chiplet and heterogeneous integration developments are emerging to push technology boundaries and are elevating demand for innovative design flows and circuit-level simulations to accelerate complex design achievements. The IDE has been launched

by ASE to address design challenges of its VIPack platform technologies and extensively improve both design efficiency and quality in parallel with shortening time-to-market for customers.

The ASE IDE workflow reduces the overall design cycle time based on two synergistic achievements:

1. ### Cross platform interaction (layout and verification):
   ASE works with industry-leading EDA tool providers to address software and format compatibility issues that can arise from operating on differing platforms. As a result, layout and verification are both essential yet time-consuming iterative processes within the design workflow. Design complexity can result in thousands of verification errors in the first design layout. Significant effort is required to resolve every error and continues throughout the entire cyclical design & verification phase. ASE has streamlined the compatibility between multiple EDA vendors to simplify the layout and verification process, which has resulted in a 50% cycle time reduction during this phase.

2. ### Advanced wafer level RDL/Si interposer auto-routing:
   By incorporating a robust auto-routing and embedded design rule check at the advanced wafer level RDL/Si interposer design layout phase, much of the task can be automated thereby reducing the cycle time by 50% accordingly. As the design process expands beyond the silicon and substrate, new methodologies to enhance electrical performance are required to address other separate routing layers created in either wafer level RDL stacks or Si interposers.
   The ASE IDE is ideal for optimizing the design of VIPack structures geared towards artificial intelligence (AI) and machine learning (ML), high-performance computing (HPC), 5G communication networks, autonomous transportation, and consumer electronics. ASE's Director of Engineering & Technical Promotion, Charles Lee, observed, "Advanced packaging helps create the magic of what is possible across today's dynamic application landscape, therefore the IDE is a crucial step forward for ASE in our endeavor to bring the most systematic package design enablement to our customers."

   "ASE's launch of the IDE elevates our package design efficiency and signifies our commitment to deliver the performance, cost, and time-to-market benefits our customers need to stay competitive," commented Dr. CP Hung, Vice President of R&D, ASE. "While ASE has been in production with 2.5D for nearly ten years, package complexity continues to rise and the new design methodologies within IDE set ASE apart."

   "Our business is built on driving the technology and innovation required to bring greater value to our customers," remarked Yin Chang, ASE's Senior Vice President of Sales & Marketing. "ASE has been extremely intentional in terms of collaborating more closely across the EDA ecosystem and helping to drive design tool improvements that are bringing unprecedented levels of performance and efficiency to advanced packaging creativity."

ASE's IDE underpins VIPack™, a scalable platform that is expanding in alignment with industry roadmaps. The IDE PDK is available upon request and under NDA.

Supporting resources

- For more about IDE, please visit: **ase.aseglobal.com/ide/**
- For more about VIPack™, please visit: **ase.aseglobal.com/vipack/**
- Follow us on our LinkedIn page for targeted updates and announcements @aseglobal
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About ASE, Inc.

ASE, Inc. is the leading global provider of semiconductor manufacturing services in assembly and test. Alongside a broad portfolio of established assembly and test technologies, ASE is also delivering innovative advanced packaging and system-in-package solutions to meet growth momentum across a broad range of end markets, including 5G, AI, Automotive, High-Performance Computing, and more. To learn about our advances in SiP, Fan-out, MEMS & Sensor, Flip Chip, and 2.5D, 3D & TSV technologies, all ultimately geared towards applications to improve lifestyle and efficiency, please visit: **aseglobal.com** or follow us on Twitter: @aseglobal.

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