Q4 Company

Cadence Digital and Custom/Analog Design Flows Achieve the Latest TSMC N2 Certification

9/27/2023

Highlights:

- Cadence digital full flow includes key new technologies, including a high-accuracy and massively scalable parasitic 3D field solver
- AI-powered Cadence Cerebrus enabled for N2 provides customers with productivity improvements
- Custom/analog flow based on AI-powered Virtuoso Studio supports circuit optimization and has been enhanced, providing up to 3X throughput for design migration
- Mutual customers actively designing with N2 PDKs to create AI, hyperscale and mobile ICs

SAN JOSE, Calif.--(BUSINESS WIRE)-- Cadence Design Systems, Inc. (Nasdaq: CDNS) today announced its digital and custom/analog flows have achieved certification for TSMC's latest N2 Design Rule Manual (DRM). Through this latest collaboration, the companies delivered new N2 process design kits (PDKs) to make it easy for customers to leverage the latest technologies from both companies, including Cadence® AI technologies that improve designer productivity. Mutual customers are already designing innovative AI, hyperscale computing and mobile applications using the N2 PDKs, accomplishing design objectives, simplified analog process migration and faster time to market.

Cadence Digital Full Flow

The complete, certified Cadence digital full flow includes the Innovus™ Implementation System, Quantus™ Extraction Solution and QuantusField Solver, Tempus™ Timing Solution and ECO Option, Pegasus™ Verification System, Liberate™ Characterization Portfolio and Voltus™ IC Power Integrity Solution. For more information on the digital full flow, visit **www.cadence.com/go/cdnsdigitalff**.

The digital full flow supports all the latest TSMC N2 PDK requirements, offering customers several key new features. In addition, the Quantus Field Solver offers process modeling of comprehensive geometries and parasitic effects at N2, delivering highly accurate models for SRAM, memory, high-performance and sensitive designs. The Innovus Implementation System engines have been enhanced to achieve N2 design goals with optimal utilization, based on a predictable, convergent flow. The Pegasus Verification System for physical signoff delivers a productivity boost through a tight integration with Cadence's Virtuoso® Studio. Finally, the Voltus IC Power Integrity Solution provides IR analysis across the frontside layers, enabling customers to build a robust power network for IR drop closure.

The Cadence Cerebrus™ Intelligent Chip Explorer is also enabled on N2, which allows customers to spend less time on manual design processes, providing productivity improvements.

Cadence Custom/Analog Flow

The Cadence custom/analog flow, certified for TSMC's N2 technology, is based on the Virtuoso Studio, which includes the Virtuoso Schematic Editor, Virtuoso ADE Suite and Virtuoso Layout Suite. Also included is the Spectre® Simulation Platform, including the Spectre X Simulator and Spectre eXtensive Partitioning Simulator (XPS). This latest flow provides a complete suite of routing technology accurately covering all custom/analog topologies. For more information on the custom/analog flow, visit **www.cadence.com/go/cdnscustomanalog**.

The new Virtuoso ADE architecture has been augmented to let users manage up to tens of thousands of simulation tests in parallel on modern compute farms and public and private clouds, all while reducing the Virtuoso memory footprint. Enhanced verification methods have been added to ensure design robustness. Spectre FMC Analysis statistical technology quickly finds tail samples that can cause design failures. Additionally, new optimization algorithms are available to swiftly recenter migrated designs to new specification tolerances.

The Virtuoso Layout Suite has also been updated for efficient layout implementation on TSMC's N2, providing performance enhancements like core editing commands, connectivity extraction, layout navigation and stream-out to abstract generation; enhanced abutment of analog cells with a track pattern assistant; a unique non-uniform grid-based, structured device placement methodology with interactive, assisted features for placement, routing, fill and insertion; device-level auto-routing to managed advanced-node complexities; automated DRM-compliant guard ring generation; integrated parasitic extraction and EM-IR checks; enhanced custom migration and reuse functionality; seamless place-and-route engine integration with Innovus Implementation System to improve quality of results (QoR).

"Through our long-time collaboration with Cadence, customers have access to our latest N2 process technology and the enhanced Cadence digital and custom/analog flows to create next-generation AI, hyperscale and mobile ICs,"said Dan Kochpatcharin, head of the Design Infrastructure Management Division at TSMC. "Cadence and TSMC

worked closely with customers to understand their most pressing design needs so we could fine-tune our solutions to best meet their requirements and enable them to accelerate time to market."

"We continue to be deeply focused on innovation, and through our latest collaboration with TSMC, we've added even more new functionality to our latest certified digital and custom/analog flows to enable our customers to be successful with N2 designs," said Dr. Chin-Chi Teng, senior vice president and general manager in the Digital & Signoff Group at Cadence. "Additionally, our AI-powered solutions, Cadence Cerebrus and Virtuoso Studio, offer customers innovative automation capabilities to make them much more efficient. We look forward to seeing our mutual customers achieve their design goals so they can deliver high-quality designs to market faster."

The Cadence digital and custom/analog flows support the Cadence Intelligent System Design™ strategy, enabling customers to achieve system-on-chip (SoC) design excellence. To learn more about Cadence's advanced-node solutions, visit **www.cadence.com/go/advndn2pr**.

About Cadence

Cadence is a pivotal leader in electronic systems design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. Cadence customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic market applications, including hyperscale computing, 5G communications, automotive, mobile, aerospace, consumer, industrial and healthcare. For nine years in a row, Fortune magazine has named Cadence one of the 100 Best Companies to Work For. Learn more at **cadence.com**.

Category: Featured

For more information, please contact:

Cadence Newsroom

408-944-7039

newsroom@cadence.com

Source: Cadence Design Systems, Inc.