NEWS RELEASE

Cadence Expands Support for 3Dblox 2.0 Standard with New System Prototyping Flows

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Highlights:

- Cadence Integrity 3D-IC Platform fully supports latest 3Dblox 2.0 standard across all TSMC's 3DFabric offerings
- Integrity 3D-IC Platform uniquely combines system planning, implementation and system-level analysis in a single solution, enabling seamless prototyping
- Mutual customers creating AI, mobile, 5G, hyperscale computing and IoT 3D-IC designs can model system prototypes to accelerate multi-chiplet design turnaround time

SAN JOSE, Calif.--(BUSINESS WIRE)-- Cadence Design Systems, Inc. (Nasdaq: CDNS) today announced the availability of new system prototyping flows based on the Cadence® Integrity™ 3D-IC Platform that support the 3Dblox 2.0 standard. The Integrity 3D-IC Platform is fully compliant with the 3Dblox 2.0 standard language extensions, and the flows have been optimized for all of TSMC's latest **3DFabric™** offerings, including Integrated Fan-Out (InFO), Chip-on-Wafer-on-Substrate (CoWoS®) and System-on-Integrated-Chips (TSMC-SoIC®) technologies. Through this latest collaboration between Cadence and TSMC, customers creating AI, mobile, 5G, hyperscale computing and IoT 3D-IC designs can model system prototypes to accelerate design turnaround time.

Prototyping requires two different types of feasibility-checking methods across the various 3DFabric technologies—coarse-grained feasibility for thermal and EM-IR analysis, and fine-grained feasibility for die-to-die connections.Coarse-grained feasibility is enabled through a system-level tool integration with the Integrity 3D-IC Platform, featuring Voltus™ IC Power Integrity Solution and Celsius™ Thermal Solver, providing seamless prototyping for all TSMC's latest 3DFabric configurations.Fine-grained feasibility is enabled through a silicon routing

solution as well as joint collaboration on the development of a next-generation auto-router for 3DFabric technologies, which includes performance-boosting prototyping capabilities that support TSMC's InFO and CoWoS offerings, enabled through the Integrity 3D-IC platform.

The Integrity 3D-IC platform is certified for use with TSMC's 3DFabric and the 3Dblox 2.0 specification. The platform combines system planning, implementation and system-level analysis in a single platform, and due to the shared infrastructure between Cadence 3D design and system analysis tools, customers can perform feasibility-checking much more efficiently. In addition, Cadence Allegro® X packaging solutions have been enhanced with advanced InFO-specific design rule checking (DRC).

The flows supporting the 3Dblox 2.0 standard provide chiplet mirroring, which lets engineers reuse chiplet module data, improving productivity and performance. In addition, the flows provide inter-chiplet DRC through the Cadence Pegasus™ Verification System, which helps designers create an inter-chiplet CAD layer for DRC automatically.

"With multiple packaging options available for implementation of multi-die designs, early prototyping and feasibility studies are becoming increasingly important," said Dan Kochpatcharin, head of the Design Infrastructure Management Division at TSMC. "Through our continued collaboration with Cadence and with the addition of the latest prototyping features that support the 3Dblox 2.0 standard, we're enabling customers to leverage our comprehensive 3DFabric technologies and the Cadence flows to significantly improve 3D-IC design productivity and time to market."

"The Cadence Integrity 3D-IC Platform is the unified solution that provides an efficient way for customers to leverage the new 3Dblox 2.0 prototyping capabilities to create leading-edge 3D-IC designs using TSMC's 3DFabric technologies," said Dr. Chin-Chi Teng, senior vice president and general manager in the Digital & Signoff Group at Cadence. "By working closely with TSMC, customers adopting our new flows for use with 3Dblox 2.0 standard can accelerate the pace of innovation with next-generation multi-chiplet designs."

The Cadence Integrity 3D-IC Platform includes Allegro X packaging technologies and is part of the company's broader 3D-IC offering. The offering aligns with the Cadence Intelligent System Design™ strategy, enabling customers to achieve system-in-package (SiP) design excellence. For more information on the Integrity 3D-IC platform, please visit **www.cadence.com/go/integrity3dblox2**.

About Cadence

Cadence is a pivotal leader in electronic systems design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. Cadence customers are the world's most innovative

companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic market applications, including hyperscale computing, 5G communications, automotive, mobile, aerospace, consumer, industrial and healthcare. For nine years in a row, Fortune magazine has named Cadence one of the 100 Best Companies to Work For. Learn more at **cadence.com**.

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