NEWS RELEASE

JEDEC Publishes Essential Test Method to Address Switching Energy Loss in Wide Bandgap and Silicon Semiconductor Power Devices

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ARLINGTON, Va.--(BUSINESS WIRE)-- **JEDEC Solid State Technology Association** , the global leader in the development of standards for the microelectronics industry, today announced the publication of JEP200: Test Methods for Switching Energy Loss Associated with Output Capacitance Hysteresis in Semiconductor Power Devices. Developed jointly by JEDEC's JC-70.1 Gallium Nitride and JC-70.2 Silicon Carbide Subcommittees, JEP200 is available for free download from the **JEDEC website** .

Proliferation of soft switching power conversion topologies brought about the need to accurately quantify the energy stored in a power device's output capacitance because the energy impacts efficiency of power converters. JEP200, developed in collaboration with academia, addresses the critical power supply industry need to properly test and measure the switching energy loss due to the output capacitance hysteresis in semiconductor power devices and details tests circuits, measurement methods, and data extraction algorithms. The document applies not only to wide bandgap power semiconductors such as GaN and SiC, but also silicon power transistors and diodes.

"Professionals in high-frequency power conversion systems have long sought a standardized approach to testing new switching energy losses," said Dr. Jaume Roig, Member of Technical Staff, onsemi and Vice Chair of the JC-70 Committee. "This document now provides helpful guidance on testing energy losses related to output capacitance hysteresis caused by displacement currents. With this clarity, system optimization can proceed more accurately."

"JEDEC's JC-70 committee has the expertise necessary to meet the demands of the entire power semiconductor industry, and the development of JEP200 demonstrates how the JEDEC process enabled the committee to swiftly

respond to an industry need," said John Kelly, JEDEC President. "JEP200 encompasses GaN, SiC, and Si power devices, helping the industry navigate design challenges caused by the growing number of new power conversion topologies."

Interested companies worldwide are welcome to join JEDEC to participate in the important work of the JC-70 committee. The next committee meeting will be held on November 6, 2024 in conjunction with the WiPDA conference in Dayton, Ohio. Contact Emily Desjardins (**emilyd@jedec.org**) for more information or visit **www.jedec.org** .

About JC-70

Formed in October 2017 with 23 member companies, JC-70 now has over 80 member companies, which underscores industry commitment to the development of universal standards to help advance the adoption of wide bandgap (WBG) power technologies. Global multinational corporations and technology startups from the US, Europe, Middle East, and Asia are working together to bring to the industry a set of standards for reliability, testing, and parametrics of WBG power semiconductors. Committee members include industry leaders in power GaN and SiC semiconductors, as well as users of wide bandgap power devices, and test and measurement equipment suppliers. Technical experts from universities and national labs also provide input.

About JEDEC

JEDEC is the global leader in the development of standards for the microelectronics industry. Thousands of volunteers representing over 350 member companies work together with more than 100 JEDEC committees and task groups to meet the needs of every segment of the industry, for manufacturers and consumers alike. The publications and standards generated by JEDEC committees are accepted throughout the world. All JEDEC standards are available for download from the JEDEC website. For more information, visit **https://www.jedec.org** .

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Source: JEDEC