NEWS RELEASE

OpenHW Group Announces CORE-V CVA6 Platform Project for RISC-V Software Development & Testing

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Platform Aims to Advance RISC-V Software Development Through Vendor-Neutral Open Collaboration

SANTA CLARA, Calif.--(BUSINESS WIRE)-- Today, at the RISC-V Summit, the **OpenHW Group** announced the multi-member **CORE-V CVA6 Platform project**. The platform is an open-source FPGA-based software development and testing environment for RISC-V processors designed to provide a vendor-neutral environment for RISC-V software CI and testing that keeps pace with RISC-V standards.

The CVA6 Platform initiative will unlock numerous benefits for the RISC-V community while accelerating innovation on open hardware.

As part of the project mandate, the CVA6 Platform will offer both client and server-compliant open-source processor designs, a big step towards creating a more standardized and streamlined environment. Initially the platform will target client applications, and later, expand into server applications. The CVA6 Platform is built using the CV-Mesh clustering Network-on-Chip (NoC) which is based on the OpenPiton system and P-Mesh coherence protocol, originally developed at Princeton University. The CV-Mesh NoC allows for coherent scaling of hundreds of CVA6 cores and reuses various communication interfaces between cores, caches, and memory, which speeds and smooths integration and testing of various CVA6 Platform configurations.

Hosted on Digilent Genesys2 FPGA boards, demonstrations of the CVA6 Platform running RISC-V Fedora Linux on coherent dual core CVA6 clusters will be on display at the **RISC-V Summit** in Santa Clara, Calif. the 7th & 8th of November, 2023.

Futureproofing for standards

One of the key advantages of the CVA6 Platform – based on the 64-bit open-source CORE-V CVA6 application-class RISC-V CPU – is its upgradability. The CVA6 Platform is built to evolve in response to the ever-shifting landscape of RISC-V standards. This dynamic approach unlocks the potential of hardware and software co-design and ensures the CVA6 Platform remains current and relevant, addressing emerging issues all the while staying in sync with the rapid evolution of the RISC-V ISA Specifications.

The CVA6 Platform implementation using FPGA-based hardware emulation, provides for system level silicon logic equivalence as opposed to an interpreted software simulator. This approach ensures the CVA6 Platform is firmly grounded in hardware, offering SW development teams a more robust testing environment with logic equivalence to silicon implementations.

A range of FPGA configurations will be available initially as part of the CVA6 Platform project, including:

- The CVA6 Platform on Amazon AWS EC2 F1 instances will enable SW testing on the octal CVA6 cluster in the cloud;
- Digilent Genesys 2 and Nexys Video boards provide a low-cost entry point for basic testing with 1-2 CVA6 cores in a bench top environment; and
- Other configurations such as: Xilinx VC707 boards which can support 1-4 CVA6 cores; Xilinx VCU118 and BittWare XUPP3R boards which can support around 8-10 CVA6 cores; and Xilinx Alveo U200 and U250 boards which can support significantly more CVA6 cores (~15) to enable testing of larger parallel/distributed software on many core systems are also being considered as part of the project.

Participating Company Quotes

Ashling

“Ashling, as a long-term OpenHW member, is looking forward to bringing our CORE-V SDK expertise to the CVA6 Platform. We are leading the OpenHW software SDK effort which includes an IDE, Debugger, and Compiler (from our partner and fellow OpenHW member Embecosm) with an overriding goal of elevating RISC-V based development on the CVA6 Platform to new heights," said Hugh O’Keeffe, CEO of Ashling.

Barcelona Supercomputing Center (BSC)

"As a leader in driving RISC-V adoption in Europe, BSC is honored to bring our expertise in open-source hardware components, high-performance interconnects and memory systems to the new CORE-V CVA6 Platform project. Together with the OpenHW community, we will empower the RISC-V ecosystem to advance software development

and compliance testing," said Miquel Moreto, Group Leader, High Performance Domain-Specific Architectures, BSC and Member, Board of Directors, OpenHW Group.

Red Hat

"Open standards reside at the center of successful innovations, a need that Red Hat views as an absolute necessity for widespread adoption. We're pleased to work with other industry leaders on the CORE-V CVA6 Platform project as we collectively work to make the platform an ideal location for RISC-V software testing and development," stated Hugh Brock, Director, Software Engineering, Red Hat.

Thales

"As a leading contributor to the RISC-V evolution and leaders of the CVA6 core project within the OpenHW community, we believe the CORE-V CVA6 Platform will accelerate community efforts on RISC-V compliance and software development. Initiatives like this will continue driving RISC-V adoption across markets requiring high reliability, safety, and security. Thales remains committed to the CVA6 core project, a major pillar of its strategy of core sovereignty," said Daniel Glazman, VP Software Technologies, Thales.

UCSB

"As a leader in open-source processor research and development, UCSB is excited to lead the new CORE-V CVA6 Platform project," said Jonathan Balkind, Assistant Professor at UCSB. "As evidenced by our longtime collaboration with the Princeton University OpenPiton project and our work on the CVA6 development team, UCSB is committed to open architectures that empower innovation."

The CORE-V CVA6 Platform demonstrates the power of open collaboration to drive technology innovation. By providing an open-source, community-driven environment for RISC-V software testing and development, the Platform aims to foster continued momentum for the RISC-V ecosystem.

With its flexible and scalable FPGA-based architecture, upgradability to keep pace with standards, and support from leading technology companies, the CVA6 Platform sets the stage to advance RISC-V progress for years to come. Through strategic initiatives like this, the promise of open architectures can be fully realized.

About OpenHW Group

The charter of the OpenHW Group is to develop, verify and provide open-source processor cores, along with hardware and software needed for use in high volume SoC production. OpenHW provides an infrastructure for

hosting high quality open-source HW developments in line with industry best practices. The OpenHW Cores Task Group within the organization has the mandate to develop the open-source IP for the CORE-V family of open-source RISC-V processors. The OpenHW Group is a global, non-profit, member-driven organization based in Canada, and partnered with the Eclipse Foundation.

Media Contact for the OpenHW Group:

Michelle Clancy Fuller
+1 503-702-4732
michelle@openhwgroup.org

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